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EXAMINER	
DESTA, ELIAS	
ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/552,117	UDUMAN, BOGDAN M
Examiner	**Art Unit**
Elias Desta	2857

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If the period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Detailed Action

Claim rejection - 35 U.S.C 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. *Claims 1-15* are rejected under 35 U.S.C. 102 (a) as being unpatentable over *National LM2637*

In reference to claims 1, 6 and 11: *National LM2637* datasheet teaches an integrated circuit for monitoring and controlling multiple power outputs from a power supply (ATX not shown) that generates a primary power voltage (Vcc), and one more secondary power voltage (V_{DD}) derived from the primary power voltage (see *National LM2637* Fig. 2, and page 8-9 application information). *National LM2637* has an input means for receiving the primary and secondary power voltages from the power supply (see Pin Description in page 8). The integrated circuit has a means for controlling the primary and secondary power voltages to generate controlled voltage power outputs (see *National LM2637* page 8, pin 16-20, and overview first paragraph).

In page 2 of *National LM2637*, the integrated circuit consists of threshold variables ($V_{CC\text{-}TH1}$ and $V_{CC\text{-}TH2}$) with corresponding limit values for the primary power source. The threshold variables and the limiting values constitute a means for sensing when the primary power voltage reaches or exceeds a threshold reference level. Further, the *National LM2637* also has a means for delaying connection of the primary and secondary power voltages to the controlled voltage power outputs for selected delay time after

the primary power voltage reaches the reference threshold level. (See page 8, theory of operation, start up, first paragraph.)

With regard to claims 2, 7 and 12: the *National LM2637* has a means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a useable and effective voltage level through 'Over Voltage Protection' output signal. (See page 8, pin 11, and 'over voltage protection', page 9 to 10).

With regard to claims 3, 8 and 13: *National LM2637* has a means for comparing includes a voltage divider (see page 5, Fig. 1 pin number 21 and 22 where V_{CC} is supplied to EA, and two resistors with 35.2 and 36 kΩ are used as a voltage divider where SNS3 is one of the output voltages), and a comparator (also shown in page 5, Fig. 1, labeled as 'UV3'). Since one input of UV3 is tied to a threshold 0.63 volt, it implies that the threshold reference voltage, and the comparator 'UV3' are coupled together. Further more, the voltage divider is coupled through the comparator logic, and current limiting circuit, which shows the voltage divider, is coupled to the primary power voltage and to the comparator.

With regard to claims 4 and 9: the *National LM2637* has a delaying means that consist of a timing circuit (see page 5, Fig. 1, an oscillator with a clock generator, and clock input to the logic block), and the output of the comparator is coupled to the timing circuit for delaying connection of the input power supply voltages to the controlled outputs for the selected delay time (see Fig. 1, and 'Theory of Operation' pages 8 and 9).

With regard to claims 5, 10 and 15: the *National LM2637* has a linear controller for controlling the output voltage of each of the power output voltages of the power monitor circuit (see 'under-voltage latch-off' discussion on page 10). Further, *National LM2637* also has two linear controllers with each linear

controller controlling voltage of one of the power output voltages of the power monitor circuit. (See page 8, 2nd column, under 'linear section'.)

With regard to claim 14: the *National LM2637* datasheet teaches the comparator means has a timing circuit (see Fig.1, pin 12 and 13, the same ramp clock signal) that is used to time an interval starting when the voltage divided signal exceeds the threshold reference signal and delaying connection of the controlled voltage power outputs to the computer for selected delay time (see page 9-10, 'over-voltage protection').

Examination of New Claims

Specification

3. The specification is objected to because of the following minor informalities

- Page 3, line 9: "to exacting specification" should rather read "to exact specification";
- Page 3, line 17: " ... one input pin that provide" should rather read " ... one input pin that provides".

Claim rejection – 35 U.S.C. 102

4. *Claims 16-25* are rejected under 35 U.S.C. 102 (a) as being unpatentable over *National LM2637*

In reference to claim 16: as noted above in claims 1, 6 and 11, *National LM2637* datasheet teaches a power monitoring circuit (see Fig. 2, pages 8-9). The circuit consists of:

- A primary input adapted to receive a primary voltage from a power supply (see port V_{cc} in Fig. 2);

- One more secondary input to receive one or more secondary voltages from the power supply, wherein the one or more secondary voltages are derived from the primary voltage (such as 3.3, 5 and 12 volts, as shown in Fig. 3);
- A comparator circuit adapted to compare the primary voltage with the reference voltage (see Fig. 4);
- It is inherent that a time delay circuit is adapted to delay an output of the secondary voltages by a select period once the primary voltage equals or exceeds the reference voltage, because soft-start time 4096 cycles or ranges from 4.1 to 82 ms depending on the clock frequency (50KHz to 1MHz.) (See pages 9-10 Switching section, over-voltage protection and page 4, DAC output voltage table).

With regard to claim 17: as noted above in claim 16, National LM2637 further shows that comparator circuit includes:

- A resistor divider network adapted to divide the primary voltage, the resistor divider network consists of:
  - A first resistor of a first select value (see Fig. 1, R = 36 kΩ network, and
  - A second resistor of second select value, and first and second resistor being adapted to divide the primary voltage into a select divided primary voltage (see Fig. 1, R = 35.2 kΩ with port 22); and
- A comparator having a first input coupled to the resistor divider network to receive the select divided primary voltage, the comparator having a second input coupled to receive the reference voltage (see Fig. 4), but National LM2637 does not show in Fig. 1 or 4 as the comparator further having an output coupled to the time delay circuit; however, the theory

of operation in pages 8-9 indicates that the system should have to have a delay circuit when the power supply when the chip goes through a soft start process before the output voltages show the appropriate digital logic voltage level is detected.

With regard to claim 18: as noted above in claim 16, National LM2637 further shows that the reference voltage is approximately equal to 90% of the primary voltage (see page 9, "Power Good Signal").

With regard to claim 19: as noted above in claim 16, National LM2637 further shows that the time delay circuit outputs the primary and one more secondary voltage approximately between 4.1 to 82 ms, hence an approximation of 40 ms would fall with in the range after the primary voltage equals or exceeds the reference voltage (see pages 9-10, Switching, Over Voltage Protection sections, and page 4, DAC output voltage table).

With regard to claim 20: as noted above in claim 16, National LM2637 further shows that the primary voltage is approximately equal to 12 volts and 5 volts, and one of the secondary voltages is approximately equal to 3.3 volt (see Fig. 3; 5 and 3.3 volt ports). Neither the claimed invention nor National LM2637 discloses a single primary source.

In reference to claim 21: as noted above in claims 1, 6, 11 and 16, National LM2637 teaches a power monitor circuit for monitoring two or more voltages from a power supply where the power supply derives the two or more voltages from a single voltage (see pages 1 and 6), the power monitor circuit includes:

- A first input adapted to receive one voltage of the two or more voltages from the power supply (see Fig. 2);

- A secondary input for each of the remaining two or more voltages, each secondary input adapted to receive an associated one of the remaining two or more voltages (see Fig. 2, ports v2 and v3);
- An output for each of the two or more voltages (see Fig. 3; 3.3, 5 and 12 volts);
- A comparator circuit adapted to compare the one voltage received at the first input with a reference voltage; and
- A time delay circuit adapted to delay the coupling of the two or more voltages to the outputs for a selected period after the comparator has sensed the one voltage received on the first input equals or exceeds the reference voltage (see pages 8-9, theory of start up).

With regard to claim 22: as noted above in claim 21, National LM2637 further shows that the one or two voltage received on the first input are primary voltage and the remaining two or more voltages are secondary voltages derived from the primary voltage; however, applicant's claim assertion that all secondary voltages are derived from a single source is not supported by applicant's disclosed figures; for instance, Fig. 1 of the application shows three primary sources and one stand by voltage, and the voltage divider arrangement is followed from one of the primary voltages, labeled as V12.

With regard to claim 23: as noted above in claim 21, National LM2637 further shows that the resistance voltage is in relation to 90% of the nominal setting of the one voltage received at the first input (see page 9, "Power Good Signal").

With regard to claim 24: as noted above in claim 21, National LM2637 further shows that the selected period is approximately between 4.1 and 82 ms, hence an approximation of 40 ms would fall with in the range after the primary voltage equals or exceeds the reference voltage (see pages 9-10, Switching, Over Voltage Protection sections, and page 4, DAC output voltage table).

With regard to claim 25: as noted above in claim 21, National LM2637 further includes a voltage divider adapted to provide the one voltage received on the first input, where the divided one voltage received on the first input, where the divided one voltage received on the first input is compared to the reference voltage (see Fig. 4).

Response to Argument

5. *In reference to 1, 6 and 11*: Unlike the applicants' assertion, *National LM2637* teaches a means for delaying connection of the primary and secondary power voltages to the controlled voltage outputs for a selected delay time after the primary power voltages reach the reference threshold level (see pages 8-9, Theory of Operation, Start up).

The primary voltage, as disclosed in Fig. 1 of the claimed invention, consists of three primary voltages, namely 3.3, 5 and 12 volts; hence, the claimed invention measures the primary voltages, which is consistent with National LM2637 specification. If claim 1 reads into a primary voltage source as a single, 12-volt source, then Fig. 1 of the claimed invention fails to disclose the right feature.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory

action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Desta whose telephone number is (703)-305-3840. The examiner can normally be reached on M-Thu (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)-308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-5841 for regular communications and (703)-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-1782.

Elias Desta
Examiner
Art Unit 2857

-ed

February 3, 2003

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
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